XA-9590
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Masao SHINOZAKI et al.

Serial No.: 10/002,009 Group Art Unit: 2814

Filed: December 5, 2001 Examiner: S. Rao

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

Allowed: October 16, 2003

Confirmation No.: 3040

* * *

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Attn: Mail Stop Issue Fee

Sir:

Applicants wish to point out that the Examiner's Statement of Reasons for Allowance regarding "spacing" specifically addresses recitations of allowed Claim 1, but not allowed Claim 2. Claim 2 recites "spacing between an edge of a first active region in which the first MOS transistors are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a spacing between an edge of a second active r gion in which the second MOS

transistors are formed and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors".

The Reasons for Allowance of Claim 2 are apparent in the argument on pages 10 and 11 of the Amendment dated August 4, 2003.

Respectfully submitted,

NHS:lmb

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January 16, 2004